



PRTR5V0U2X-Q

Ultra low capacitance double rail-to-rail ESD protection diode

4 May 2022

Product data sheet

1. General description

Ultra low capacitance rail-to-rail ElectroStatic Discharge (ESD) protection diode in a small SOT143B Surface-Mounted Device (SMD) plastic package designed to protect two Hi-Speed data lines or high-frequency signal lines from the damage caused by ESD and other transients.

PRTR5V0U2X-Q incorporates two pairs of ultra low capacitance rail-to-rail diodes as well as an additional ESD protection diode to ensure signal line protection even if no supply voltage is available.

2. Features and benefits

- ESD protection of two Hi-Speed data lines or high-frequency signal lines
- Ultra low input/output to ground capacitance: $C_{(I/O-GND)} = 1 \text{ pF}$
- ESD protection up to 8 kV
- IEC 61000-4-2, level 4 (ESD)
- Very low clamping voltage due to an integrated additional ESD protection diode
- Very low reverse current
- Small SMD plastic package
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- USB 2.0 ports
- Digital Video Interface (DVI) / High Definition Multimedia Interface (HDMI) interfaces
- Mobile and cordless phones
- Personal Digital Assistants (PDA)
- Digital cameras
- Wide Area Network (WAN) / Local Area Network (LAN) systems
- PCs, notebooks, printers and other PC peripherals

4. Quick reference data

Table 1. Quick reference data

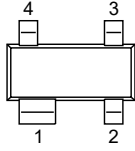
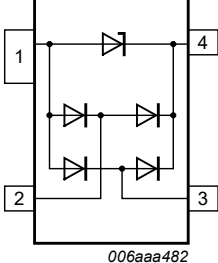
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|------------------------------------|---|-----|-----|-----|------|
| V_{RWM} | reverse standoff voltage | | - | - | 5.5 | V |
| $C_{(I/O-GND)}$ | input/output to ground capacitance | $f = 1 \text{ MHz}; V_{(I/O-GND)} = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$ [1] | - | 1 | 1.5 | pF |
| C_{sup} | supply pin to ground capacitance | $f = 1 \text{ MHz}; V_{cc} = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$ [2] | - | 16 | - | pF |

[1] Measured from pin 2 and 3 to ground.

[2] Measured from pin 4 to ground.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|-----------------|----------------|---|--|
| 1 | GND | ground |  <p>SOT143B</p> |  <p>006aaa482</p> |
| 2 | I/O 1 | input/output 1 | | |
| 3 | I/O 2 | input/output 2 | | |
| 4 | V _{CC} | supply voltage | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|---------|--|---------|
| | Name | Description | Version |
| PRTR5V0U2X-Q | SOT143B | plastic, surface-mounted package; 4 leads; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body | SOT143B |

7. Marking

Table 4. Marking codes

| Type number | Marking code ^[1] |
|--------------|-----------------------------|
| PRTR5V0U2X-Q | %R1 |

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------------------|---------------------------------|----------------------------------|-----|-----|------|
| V_{RWM} | reverse standoff voltage | | - | 5.5 | V |
| T_{amb} | ambient temperature | | -40 | 85 | °C |
| T_{stg} | storage temperature | | -55 | 125 | °C |
| ESD standards compliance | | | | | |
| V_{ESD} | electrostatic discharge voltage | IEC 61000-4-2; contact discharge | -8 | 8 | kV |

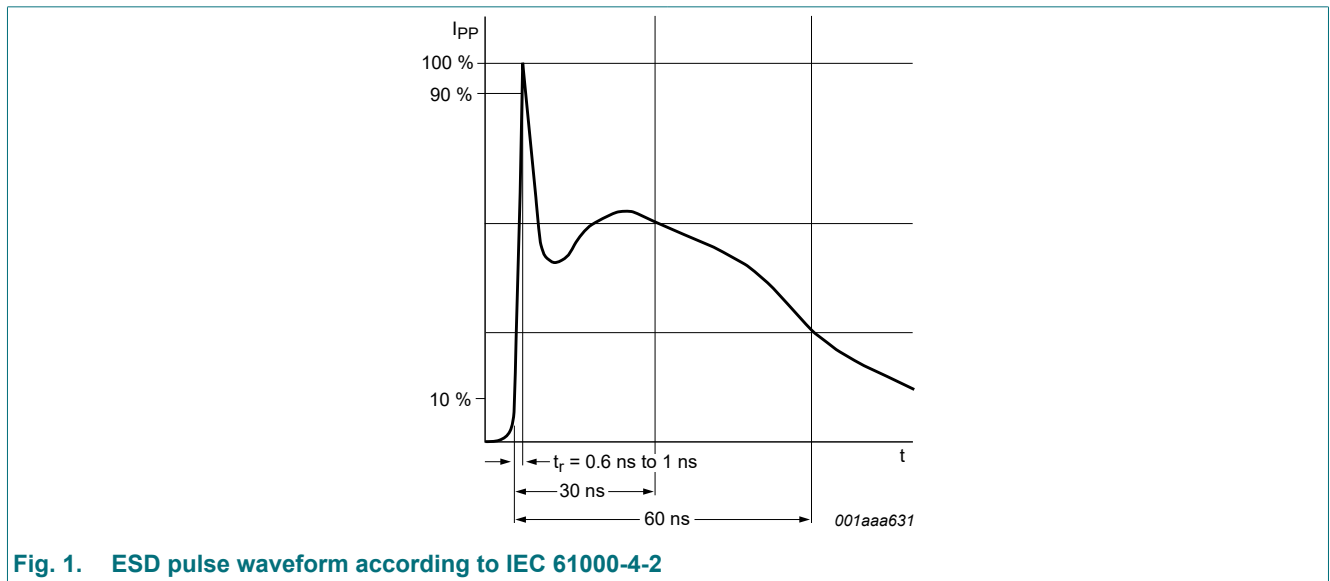


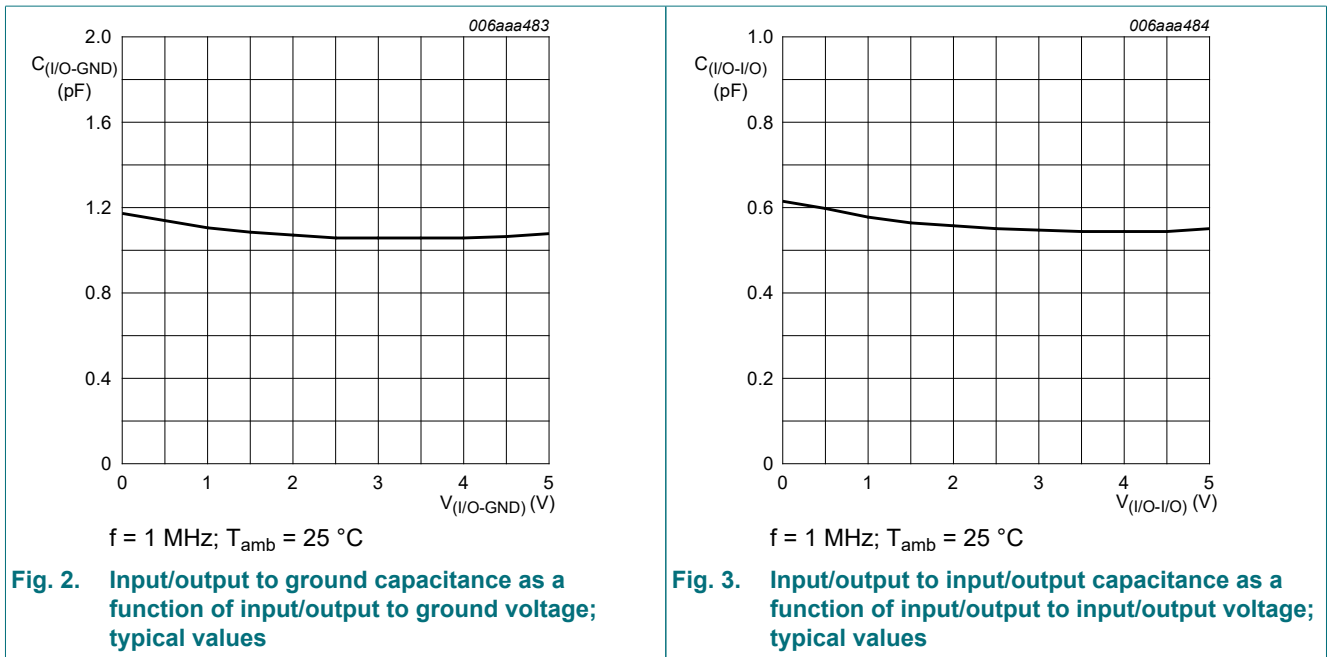
Fig. 1. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--|--|-----|-----|-----|------|
| V_F | forward voltage | $T_{amb} = 25\text{ °C}$ | - | 0.7 | - | V |
| V_{BR} | breakdown voltage | [1] | 6 | - | 9 | V |
| I_R | reverse current | $V_R = 3\text{ V}; T_{amb} = 25\text{ °C}$ | [2] | < 1 | 100 | nA |
| $C_{(I/O-GND)}$ | input/output to ground capacitance | $f = 1\text{ MHz}; V_{(I/O-GND)} = 0\text{ V}; T_{amb} = 25\text{ °C}$ | [3] | 1 | 1.5 | pF |
| $C_{(I/O-I/O)}$ | input/output to input/output capacitance | $f = 1\text{ MHz}; V_{(I/O-I/O)} = 0\text{ V}; T_{amb} = 25\text{ °C}$ | [4] | 0.6 | - | pF |
| C_{sup} | supply pin to ground capacitance | $f = 1\text{ MHz}; V_{cc} = 0\text{ V}; T_{amb} = 25\text{ °C}$ | [1] | 16 | - | pF |
| V_{CL} | clamping voltage | $I_{PPM} = 2.5\text{ A}; 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ °C}$ | [5] | 17 | - | V |
| | | $I_{PPM} = -2.2\text{ A}; 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ °C}$ | [5] | -4 | - | V |

- [1] Measured from pin 4 to ground.
- [2] Measured from pin 2, 3 and 4 to ground.
- [3] Measured from pin 2 and 3 to ground.
- [4] Measured from pin 2 to pin 3.
- [5] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.



Ultra low capacitance double rail-to-rail ESD protection diode

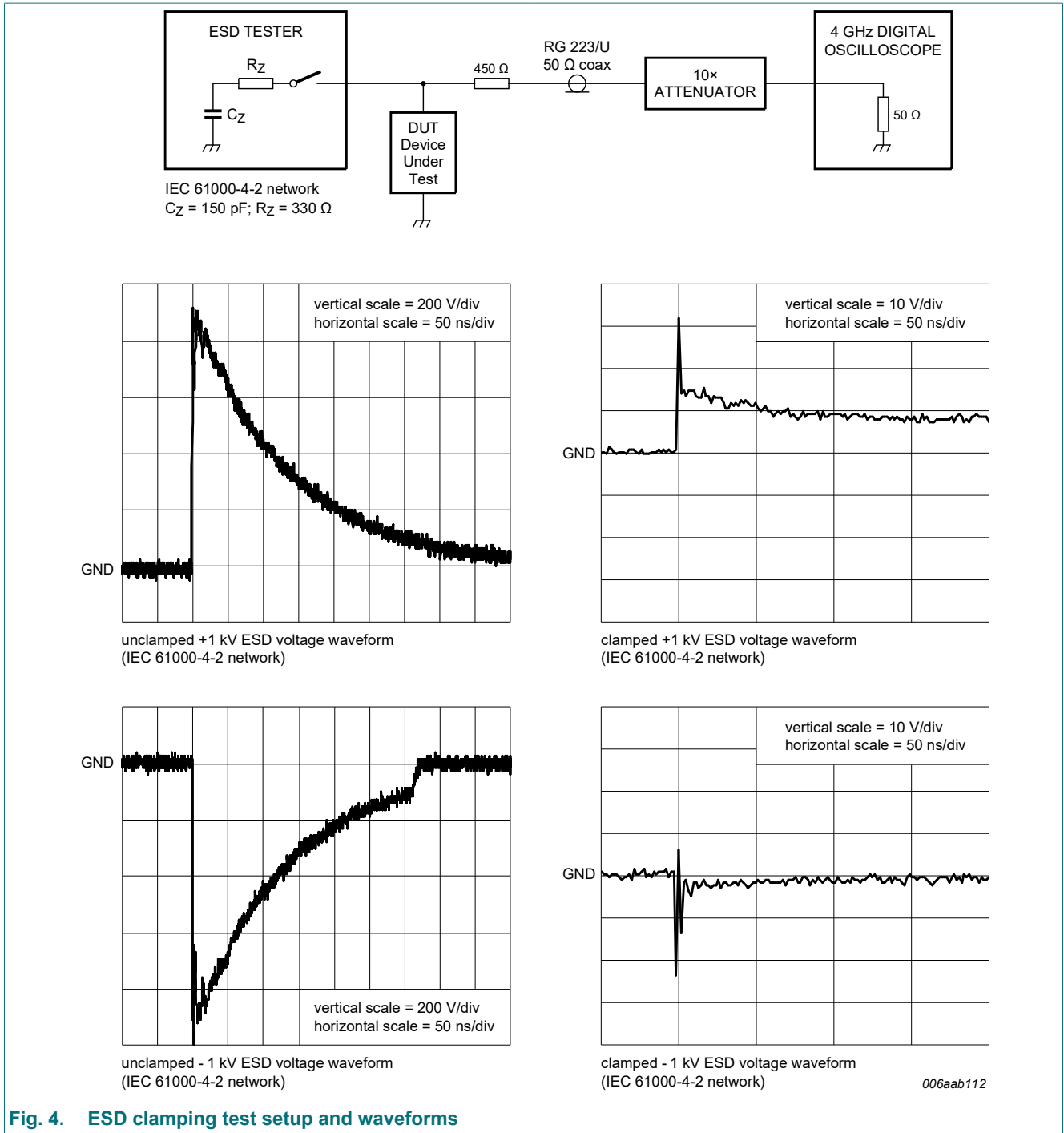


Fig. 4. ESD clamping test setup and waveforms

10. Application information

Handling data rates up to 480 Mbit/s, USB 2.0 interfaces require ESD protection devices with an extremely low line capacitance in order to avoid signal distortion.

With a capacitance of only 1 pF, the device offers IEC 61000-4-2, level 4 compliant ESD protection.

The device integrates two pairs of ultra low capacitance rail-to-rail ESD protection diodes and an additional ESD protection diode.

The additional ESD protection diode connected between ground and V_{CC} prevents charging of the supply.

To achieve the maximum ESD protection level, no additional external capacitors are required.

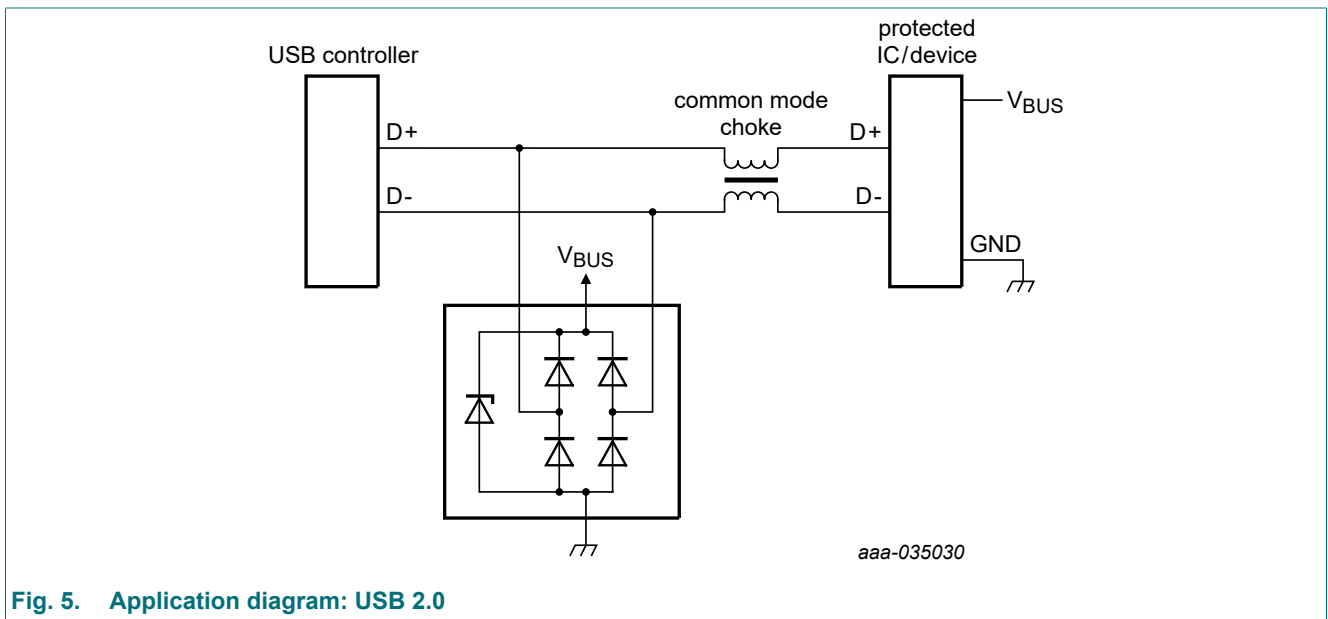


Fig. 5. Application diagram: USB 2.0

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. The path length between the device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

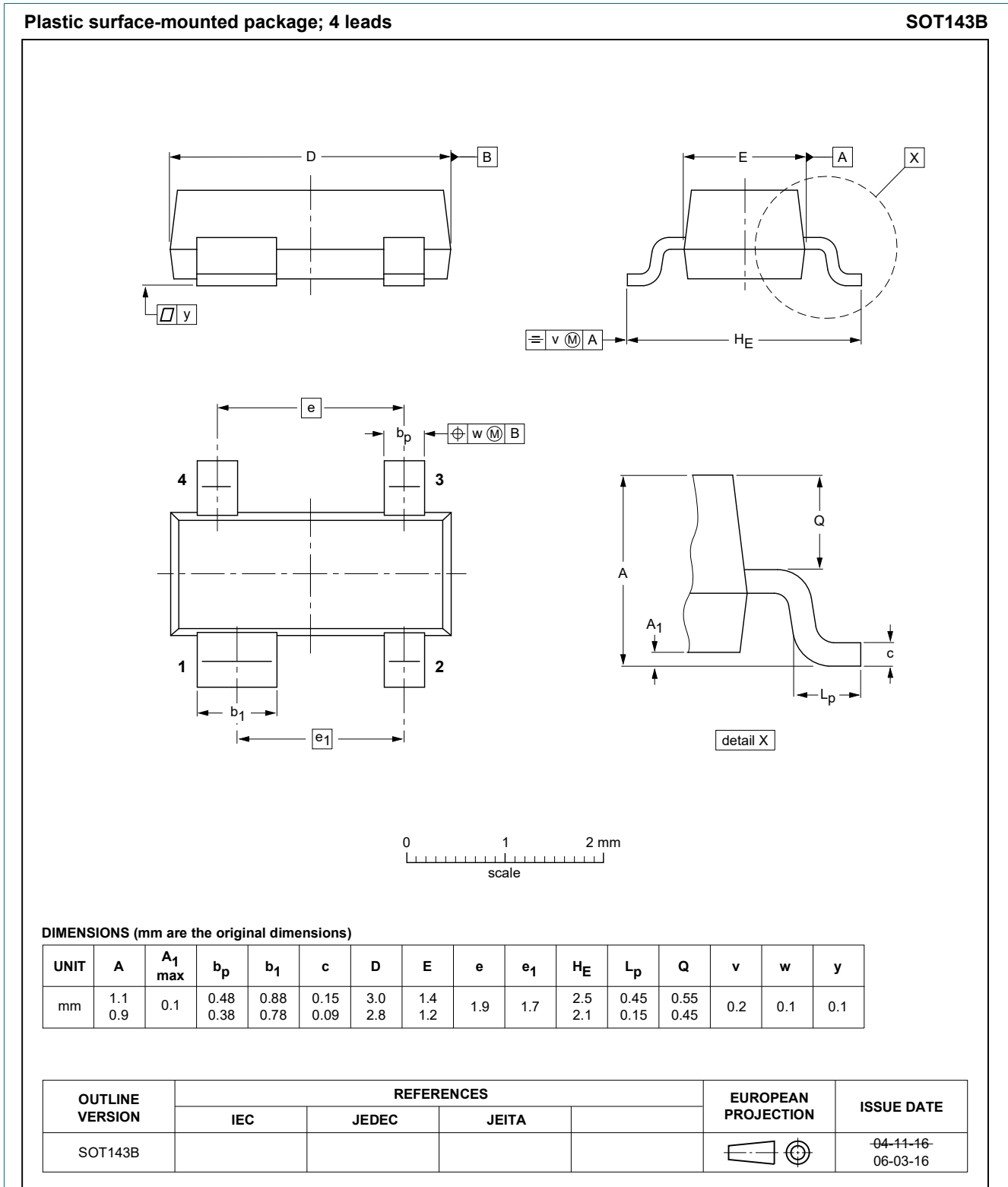


Fig. 6. Package outline SOT143B

12. Soldering

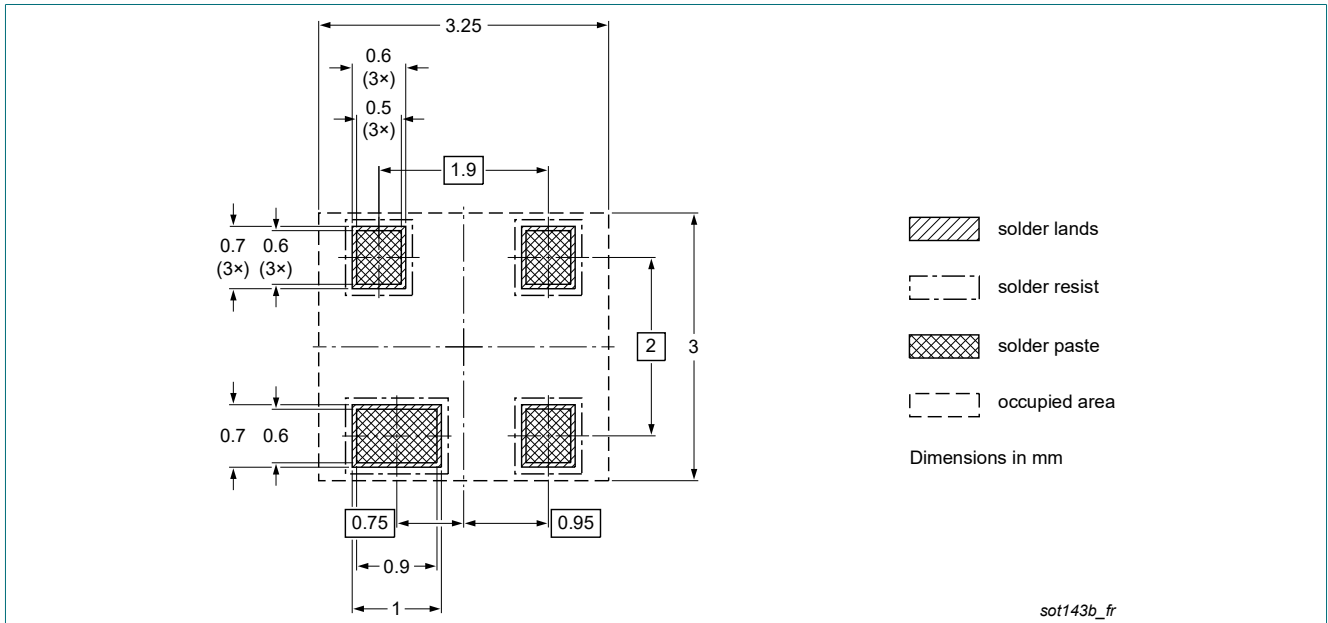


Fig. 7. Reflow soldering footprint for SOT143B

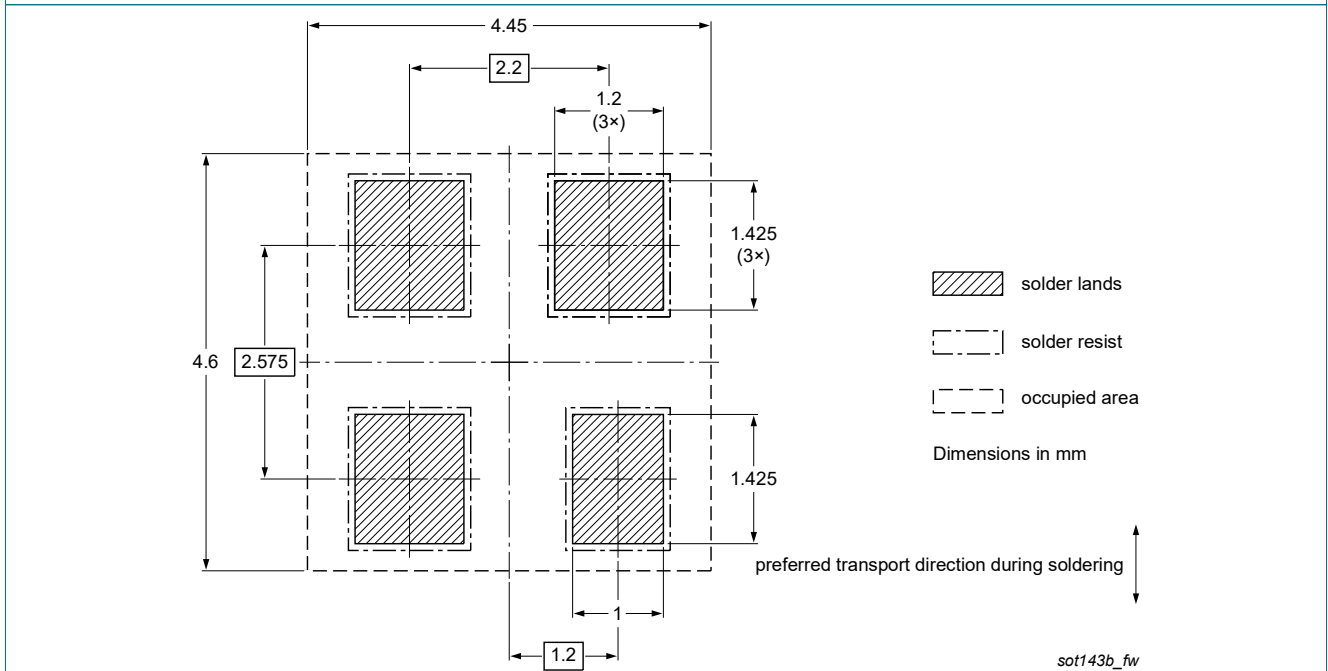


Fig. 8. Wave soldering footprint for SOT143B

13. Revision history

Table 7. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--------------|--------------------|---------------|------------|
| PRTR5V0U2X-Q v.1 | 20220504 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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